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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,263	12/30/2003	Chen-Chi Kuo	Intel-010PUS	7471

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EXAMINER

SCHLIE, PAUL W

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/751,263	KUO ET AL.
Examiner	Art Unit	
Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 30 December 2003.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-27 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-27 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 December 2003 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)              |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date 1. | 6) <input type="checkbox"/> Other: _____.  |

## DETAILED ACTION

1. Claims 1-27 have been examined.

### *Specification*

2. The specification is objected to because although a numerical algorithm as depicted in figures 3A-C is discussed, its numerical basis is insufficiently disclosed to enable its reasonable convenient examination as required in effort to ascertain its likely operability. Further detailed explanation is required, although the applicant is reminded that no new matter not supported by the original disclosure may be added.

### *Claim Rejections - 35 USC § 112*

Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure that is not enabling. As both the "predetermined number of bits" and the "predetermined offset value" are deemed critical or essential to the practice of the invention, but not included in the claims nor enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Corrective action is required, however the applicant is reminded that no new matter not supported by the original disclosure may be added.

### *Claim Rejections - 35 USC § 102/103*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-27 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Miwa et al. (3,806,881).

As per independent claims 1, 10, 14, 18 and 23, Miwa et al. teaches a system and/or method comprising: a processor, the configuration/allocation of memory potentially non-uniformly among a plurality of memory channels/module/bank, determining/decoding a logical address (which may inherently be a program address from said processor) to a physical address within a correspondingly determined memory channel/module/bank which may perform a predetermined (such as reading or writing the correspondingly determined/decoded memory location, or not otherwise determined to address a valid memory region potentially signaling such a condition) action (see column 2 lines 46-63, figure 10 depicting different sized memory channels/banks, and figure 12 depicting logical to physical channel/bank select and memory address decode); but does not teach that said processor may be a network processor, however official notice is given that it is considered inherent that such a system may comprise any type of known processor regardless of its functional role, thereby obvious to one of ordinary skill in the art to combine that taught by Miwa et al. relevant to the claims with that considered obvious, for the benefit of composing a network processing system comprising a network processor to composed a system consisting of such memory

channels/banks. Any remaining limitation not otherwise explicitly addressed is considered correspondingly obviously inherent in that taught, clearly obvious to one of ordinary skill in the art at the time of the disclosed invention, and/or not sufficient to patentably distinguish over prior art.

As per claims 2-9, 11-13, 15-17, 19-22 and 24-27, being dependent on claim 1, 10, 14, 18, 23, or correspondingly dependent claim inclusively, Miwa et al. further teaches that memory channels/banks having the same logical amount of memory may be interleaved. Official notice is given that it is common knowledge to those of ordinary skill in the art that any arbitrary logical and/or physical memory channel/bank may be logically subdivided/allocated into/as a plurality of corresponding logical memory channel/banks and be arbitrarily mapped mutually exclusively anywhere within a given logical address space as an arithmetic function of its delimiting bounds, a logically addressed interleaved memory channel/bank is defined by the arithmetic formula

$$\text{channel/bank} = (\text{interleaved\_address} / \text{interleave\_block\_size}) \bmod \text{interleaved\_banks},$$

where interleaved\_address represents the decoded logical address of a logical region of memory whose address is both interleaved and mutually exclusively distinct from other potentially allocated addressable logical memory regions, and a corresponding physical memory address of such an interleaved address is defined as physical\_address = interleaved\_address mod channel/bank; it is thereby correspondingly inherent that any algorithm which may compute these factual identities or derivative, are correspondingly obvious to one of ordinary skill in the art at the time of the claimed invention to combine with that taught by Miwa et al., for the benefit of being able to determine/decode the

Art Unit: 2186

physical channel/bank and corresponding address within that channel/bank of any arbitrarily configured/allocated potentially interleaved logical memory region potentially subdivided from a larger logical addressable memory region potentially composed itself of a plurality of physical memory channels/banks. Any limitations not otherwise explicitly addressed are correspondingly considered obviously inherent in that taught, clearly obvious to one of ordinary skill in the art, and/or not sufficient to patentably distinguish over prior art.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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